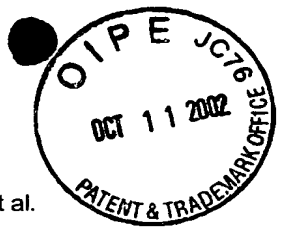
FORM PTO-1083



PATENT
Attorney Docket No. 401134/ASAHINA

In re Application of: TAKATA et al.
Application No. 09/808,151
Filed: March 15, 2001
For: SEMICONDUCTOR PACKAGE

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith is a response to an office action in the subject application.

☐ Applicants claim small entity status of this application under 37 CFR 1.27.

☒ Petition for Extension of Time
- ☐ Applicants petition for a one-month extension of time under 37 CFR 1.136, the fee for which is $110.00 (enclosed).
- ☒ Applicants believe that no petition for an extension of time is necessary. However, to the extent that such petition is deemed necessary, Applicants hereby petition for a sufficient extension of time to render the present submission timely. Please charge Deposit Account No. 12-1216 for the appropriate petition fee.

☒ No additional claim fee is required.

☒ Other: Request for Approval of Changes to the Drawings.

The claim fee has been calculated as shown below:

					Small Entity		Other Than A Small Entity	
	Claims Remaining After Amendment		Highest Number Previously Paid For	Extra Claims Present	Rate	Addit. Claim Fee	Rate	Addit. Claim Fee
Total		Minus		=	x 9=	$	x 18=	$
Independent		Minus		=	x 42=	$	x 84=	$
☐ First Presentation of Multiple Claim					+ 140=	$	+ 280=	$
					Total	$	Total	$

☐ Please charge my Deposit Account No. 12-1216 in the amount of $. A duplicate copy of this sheet is attached.

☐ A check in the amount of $ is attached.

☒ The Commissioner is hereby authorized to charge any deficiencies in the following fees associated with this communication or credit any overpayment to Deposit Account No. 12-1216. A duplicate copy of this sheet is attached.
- ☒ Any filing fees under 37 CFR 1.16 for the presentation of extra claims.
- ☒ Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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Date: October 11, 2002
JAW:ves

PATENT
Attorney Docket No. 401134/ASAHINA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKATA et al.

Application No. 09/808,151 Art Unit: 2815

Filed: March 15, 2001 Examiner: A. Wilson

For: SEMICONDUCTOR PACKAGE

AMENDMENTS TO SPECIFICATION, CLAIMS, AND ABSTRACT MADE IN RESPONSE TO OFFICE ACTION DATED JULY 17, 2002

Amendments to existing claims:

Cancel claims 1 and 8.

2. (Twice Amended) ~~The~~ A semiconductor package~~ of Claim 1, including~~ comprising:

a semiconductor chip,

a die pad,

a die bonding material fixing the semiconductor chip to the die pad,

lead-on-chip (LOC) inner leads having tips spaced from and extending across the semiconductor chip,

standard inner leads~~ and~~,

respective metal wires connecting the tips of the LOC inner leads to electrode pads on the semiconductor chip and tips of the standard inner leads to electrode pads on the semiconductor chip~~ are sealed with the~~,

a sealing resin encapsulating the semiconductor chip, the die pad, the tips of the LOC and the standard inner leads, and the metal wires, and~~ wherein~~

respective outer leads extending successively from the LOC inner leads and the standard inner leads~~ protrude~~ and protruding outwardly from the sealing resin,~~ and~~ wherein the LOC inner leads and the standard inner leads are co-planar.

3. (Twice Amended) The semiconductor package of claim ~~1~~ 2, wherein a clearance between the LOC inner leads and the die pad is larger than total thickness of the semiconductor chip and the die bond material.

6. (Twice Amended) ~~The~~ A semiconductor package ~~of claim 1,~~ comprising:

a semiconductor chip,

a die pad,

a die bonding material fixing the semiconductor chip to the die pad,

lead-on-chip (LOC) inner leads having tips spaced from and extending across the semiconductor chip,

standard inner leads,

respective metal wires connecting the tips of the LOC inner leads to electrode pads on the semiconductor chip and tips of the standard inner leads to electrode pads on the semiconductor chip,

a sealing resin encapsulating the semiconductor chip, the tips of the LOC and the standard inner leads, and the metal wires, and

respective outer leads extending successively from the LOC inner leads and the standard inner leads and protruding outwardly from the sealing resin, wherein

a distance between upper surfaces of the outer leads and an upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and a lower surface of the sealing resin, and

ends of the die pad are exposed at opposed side surfaces of the sealing resin and lie in a plane parallel to a plane in which the outer leads protrude.

PATENT
Attorney Docket No. 401134/ASAHINA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKATA et al.

Application No. 09/808,151 Art Unit: 2815

Filed: March 15, 2001 Examiner: A. Wilson

For: SEMICONDUCTOR PACKAGE

PENDING CLAIMS AFTER AMENDMENTS MADE IN RESPONSE TO OFFICE ACTION DATED JULY 17, 2002

2. A semiconductor package comprising:

a semiconductor chip,

a die pad,

a die bonding material fixing the semiconductor chip to the die pad,

lead-on-chip (LOC) inner leads having tips spaced from and extending across the semiconductor chip,

standard inner leads,

respective metal wires connecting the tips of the LOC inner leads to electrode pads on the semiconductor chip and tips of the standard inner leads to electrode pads on the semiconductor chip,

a sealing resin encapsulating the semiconductor chip, the die pad, the tips of the LOC and the standard inner leads, and the metal wires, and

respective outer leads extending successively from the LOC inner leads and the standard inner leads and protruding outwardly from the sealing resin, wherein the LOC inner leads and the standard inner leads are co-planar.

3. The semiconductor package of claim 2, wherein a clearance between the LOC inner leads and the die pad is larger than total thickness of the semiconductor chip and the die bond material.

4. The semiconductor package of claim 2, wherein the LOC inner leads and the standard inner leads are both arranged along at least one side of the semiconductor chip.

5. The semiconductor package of claim 2, wherein the LOC inner leads are arranged along a first side of the semiconductor chip and the standard inner leads are arranged along a second side of the semiconductor chip.

6. A semiconductor package comprising:

a semiconductor chip,

a die pad,

a die bonding material fixing the semiconductor chip to the die pad,

lead-on-chip (LOC) inner leads having tips spaced from and extending across the semiconductor chip,

standard inner leads,

respective metal wires connecting the tips of the LOC inner leads to electrode pads on the semiconductor chip and tips of the standard inner leads to electrode pads on the semiconductor chip,

a sealing resin encapsulating the semiconductor chip, the tips of the LOC and the standard inner leads, and the metal wires, and

respective outer leads extending successively from the LOC inner leads and the standard inner leads and protruding outwardly from the sealing resin, wherein

a distance between upper surfaces of the outer leads and an upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and a lower surface of the sealing resin, and

ends of the die pad are exposed at opposed side surfaces of the sealing resin and lie in a plane parallel to a plane in which the outer leads protrude.

7. A semiconductor package including at least a semiconductor chip, metal wires, lead-on-chip (LOC) inner leads having tips spaced from and extending over the semiconductor chip, and standard inner leads having tips arranged outside of a periphery of the semiconductor chip sealed with a sealing resin, wherein

the semiconductor chip has distributed electrode pads distributed and arranged on an upper surface of the semiconductor chip and has at least either central electrode pads rectilinearly located in a central region of the semiconductor chip or peripheral electrode pads located along the periphery of the semiconductor chip, and

the LOC inner leads and the standard inner leads are co-planar and both arranged along one side of the semiconductor chip.